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10/516,742	12/06/2004	Suk Hun Lee	3449-0407PUS1	6987

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EXAMINER	
LEE, CHEUNG	
ART UNIT	**PAPER NUMBER**
2812	

NOTIFICATION DATE	DELIVERY MODE
08/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/516,742	LEE, SUK HUN	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6-5-07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicant's Amendment and Response to the Office Action mailed on March 23, 2007 has been entered and made of record.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on June 5, 2007 was filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

3. In view of applicant's amendments and arguments filed on May 30, 2007, the rejections of claims 1-7 and 10-11 under 35 U.S.C. 103(a) as stated in the indicated Office Action have been withdrawn. Applicant's arguments have been rendered moot in view of the new or modified ground of rejection given below.

4. The indicated allowability of claims 8-9 and 12-15 is withdrawn in view of the newly discovered references to US Application No. 10/517818 and Case Law/Legal Precedent. Rejections based on the newly cited references follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shakuda (US Pub. 2002/0125492) in view of Tanizawa (US Pat. 6657234).

Referring to figures 1(a)-6 and related text, Shakuda discloses [Re claims 1 and 7] a method for fabricating a nitride semiconductor, the method comprising the step of: (a) growing a GaN-based buffer layer (23, 24) formed on a substrate 21; and (b) growing a GaN-based single crystalline layer 25 (page 2, paragraph 27; page 3, paragraph 39) on the grown GaN-based buffer layer (see fig. 1(b)), but Shakuda fails to disclose expressly wherein the GaN-based buffer layer formed in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$.

Referring to figures 1-2 and related text, Tanizawa discloses a buffer superlattice layer of $In_zGa_{1-z}N/GaN$ (col. 3, lines 56-65).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a buffer superlattice layer, as taught by Tanizawa, because it would have been to support good crystal growth and better transitions among layers of a device, thereby improving device performance.

6. Claims 2-3 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shakuda in view of Tanizawa as applied to claim 1 above, and further in view of Kano et al. (US Pub. 2001/0035531; hereinafter "Kano").

7. [Re claims 2 and 10] The combined teaching of Shakuda and Tanizawa fails to disclose expressly wherein the step (b) comprises the step of: growing an indium-doped GaN layer; growing an undoped GaN layer on the indium-doped GaN layer; and growing a silicon-doped n-GaN layer on the undoped GaN layer.

Referring to figures 1-11 and related text, Kano discloses an InGaN/AlGaN layer 50; an undoped GaN layer 6 (page 6, paragraph 87) formed on the InGaN/AlGaN layer; and a silicon-doped n-GaN layer 7 (page 7, paragraph 97, Table 2) formed on the undoped GaN layer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use doped and undoped layers before n-GaN layer, as taught by Kano, because it would have been to reduce lattice defects and to improve crystallinity (Kano, page 3, paragraph 42).

8. [Re claims 3 and 11] The combined teaching of Shakuda and Tanizawa fails to disclose expressly wherein the step (b) comprises the step of: growing an undoped GaN layer; growing an indium-doped GaN layer on the undoped GaN layer; and growing a silicon-doped n-GaN layer on the indium-doped GaN layer.

Referring to figures 1-11 and related text, Kano discloses an undoped GaN layer 3; an InGaN/AlGaN layer 30 formed on the undoped GaN layer; and a silicon-doped n-

GaN layer 7 (page 7, paragraph 97, Table 2) formed on the indium-doped GaN layer. The motivation stated in claims 2 and 10 also applies.

9. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doverspike et al. (US Pat. 6459100; hereinafter "Doverspike") in view of Tanizawa.

10. Referring to figure 1 and related text, Doverspike discloses [Re claim 4] a nitride semiconductor light emitting device comprising: a substrate 11; a GaN-based buffer layer 13 formed on the substrate; a first electrode layer of an n-GaN layer 20 formed on the GaN-based buffer layer, the silicon-doped n-GaN layer (col. 5, lines 50-55) is first electrode layer as disclosed in the specification; an activation layer 12 formed on the first electrode layer; and a second electrode layer of a p-GaN layer 23 formed on the activation layer, the Mg-doped p-GaN layer (col. 5, lines 55-65) is second electrode layer as disclosed in the specification. However, Doverspike fails to disclose expressly wherein the GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$.

Referring to figures 1-2 and related text, Tanizawa discloses a buffer superlattice layer of $In_zGa_{1-z}N/GaN$ (col. 3, lines 56-65). The motivation stated in claims 1 and 7 also applies.

11. Doverspike discloses [Re claim 5] wherein further comprising: an Indium-doped GaN layer 12 formed on the GaN-based buffer layer; and an undoped GaN layer 15 formed on the Indium-doped GaN layer (see fig. 1).

12. Doverspike discloses [Re claim 6] wherein further comprising: an undoped GaN layer 14 formed on the GaN-based buffer layer; and an Indium-doped GaN layer 12 formed on the undoped GaN layer (see fig. 1).

13. Claims 16 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Shakuda and Tanizawa as applied to claim 1 above, and further in view of Case Law/Legal Precedent.

14. Referring to figures 1(a)-6 and related text, Shakuda discloses [Re claims 16 and 18] a method for fabricating a nitride semiconductor, the method comprising the step of: (a) growing a GaN-based buffer layer (23, 24) formed on a substrate 21; and (b) growing a GaN-based single crystalline layer 25 (page 2, paragraph 27; page 3, paragraph 39) on the grown GaN-based buffer layer (see fig. 1(b)), but Shakuda fails to disclose expressly wherein the GaN-based buffer layer formed in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$, wherein the GaN-based buffer layer has a thickness of 50-800 Å.

Referring to figures 1-2 and related text, Tanizawa discloses a buffer superlattice layer of $In_zGa_{1-z}N/GaN$ (col. 3, lines 56-65). The motivation stated in claims 1 and 7 also applies.

It would have been obvious to one of ordinary skill in the art at the time of the invention because it is a matter of determining optimum process conditions by routine

experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range (see MPEP 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *Peterson*, 315 F.3d at 1330, 65 USPQ2d at 1382; *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969)).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a certain buffer thickness, because it would have been to minimize and relax the lattice mismatch without crystal defects.

15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doverspike and Tanizawa as applied to claim 4 above, and further in view of Case Law/Legal Precedent.

16. Referring to figure 1 and related text, Doverspike discloses [Re claim 17] a nitride semiconductor light emitting device comprising: a substrate 11; a GaN-based buffer layer 13 formed on the substrate; a first electrode layer of an n-GaN layer 20 formed on the GaN-based buffer layer, the silicon-doped n-GaN layer (col. 5, lines 50-55) is first electrode layer as disclosed in the specification; an activation layer 12 formed on the first electrode layer; and a second electrode layer of a p-GaN layer 23 formed on the activation layer, the Mg-doped p-GaN layer (col. 5, lines 55-65) is second electrode layer as disclosed in the specification. However, Doverspike fails to disclose expressly wherein the GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x$

≤ 1 and 0 ≤ y ≤ 1, a two-layered structure $In_xGa_{1-x}N/GaN$ where 0 < x ≤ 1, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where 0 < x ≤ 1, wherein The GaN-based buffer layer has a thickness of 50-800 Å.

Referring to figures 1-2 and related text, Tanizawa discloses a buffer superlattice layer of $In_zGa_{1-z}N/GaN$ (col. 3, lines 56-65). The motivation stated in claims 1 and 7 also applies.

It would have been obvious to one of ordinary skill in the art at the time of the invention because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range (see MPEP 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *Peterson*, 315 F.3d at 1330, 65 USPQ2d at 1382; *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969)). The motivation stated in claim 16 also applies.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

17. Claims 1 and 4-6 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3 and 15-16 of U.S. Patent No. 7193236 (hereinafter "Pat-236"). Although the conflicting claims are not identical, they are not patentably distinct from each other.

18. Pat-236 discloses [Re claim 1] a nitride semiconductor comprising: a substrate (see claim 1); a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ (see claim 3); and a GaN-based single crystalline layer on the grown GaN-based buffer layer (see claim 1).

19. Pat-236 discloses [Re claim 4] a nitride semiconductor light emitting device comprising: a substrate (see claim 15); a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ (see claim 16); a first electrode layer of an n-GaN layer formed on the GaN-based buffer layer (see claim 15); an activation layer

formed on the first electrode layer (see claim 15); and a second electrode layer of a p-GaN layer formed on the activation layer (see claim 15).

20. Pat-236 discloses [Re claim 5] wherein further comprising: an Indium-doped GaN layer formed on the GaN-based buffer layer (see claim 15); and an undoped GaN layer formed on the Indium-doped GaN layer (see claim 15).

21. Pat-236 discloses [Re claim 6] wherein further comprising: an undoped GaN layer formed on the GaN-based buffer layer (see claim 15); and an Indium-doped GaN layer formed on the undoped GaN layer (see claim 15).

22. Claims 7, 8, 12, 14 and 16-18 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 35 and 37-39 of copending Application No. 10/517818 (hereinafter "AP-818"). Although the conflicting claims are not identical, they are not patentably distinct from each other.

23. AP-818 discloses [Re claim 7] a method for fabricating a nitride semiconductor, the method comprising the step of: (a) growing a GaN-based buffer layer formed on a substrate (see claim 35) in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ (see claim 37); and (b) growing a GaN-based single crystalline layer on the grown GaN-based buffer layer (see claim 35).

24. AP-818 discloses [Re claims 8, 12, 16 and 18] a method for fabricating a nitride semiconductor, the method comprising the step of: (a) growing a GaN-based buffer

layer formed on a substrate (see claim 35) in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ (see claim 37); and (b) growing a GaN-based single crystalline layer on the grown GaN-based buffer layer (see claim 35), wherein the GaN-based buffer layer is grown in an MOCVD equipment at a temperature of 500-800°C and in a thickness of 50-800 Å by introducing sources of TMGa, TMIn and TMAl and a gas of NH_3 at the same time while supplying carrier gases of H_2 and N_2 (see claim 39).

25. AP-818 discloses [Re claims 14 and 17] a nitride semiconductor light emitting device comprising: a substrate (see claim 35); a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three layered structure $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 < x \leq 1$ (see claim 37); a first electrode layer (see claim 35) of an n-GaN layer formed on the GaN-based buffer layer (see claim 38); an activation layer formed on the first electrode layer (see claim 35); and a second electrode layer (see claim 35) of a p-GaN layer formed on the activation layer (see claim 38), wherein the GaN-based buffer layer is grown in an MOCVD equipment at a temperature of 500-800°C and in a thickness of 50-800 Å by introducing sources of TMGa, TMIn and TMAl and a gas of NH_3 at the same time while supplying carrier gases of H_2 and N_2 (see claim 39).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

26. Claims 9, 13 and 15 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 35 and 37-39 of copending Application No. 10/517818 (hereinafter "AP-818") in view of Case Law/Legal Precedent.

27. [Re claims 9, 13 and 15] AP-818 fails to disclose expressly wherein the GaN-based buffer layer is grown under a condition that flow of the sources of TMGa, TMIn and TMAl is 5-300 μmol/min and growing pressure is 100-700 torr.

It would have been obvious to one of ordinary skill in the art at the time of the invention because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species of result effective variables. These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range (see MPEP 2144.05; *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *Peterson*, 315 F.3d at 1330, 65 USPQ2d at 1382; *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969)).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a certain flow rate and pressure of sources, because it would have been to produce a buffer layer with good growth efficiency relative to the material supply amount.

This is a provisional obviousness-type double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cheung Lee

August 19, 2007

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER